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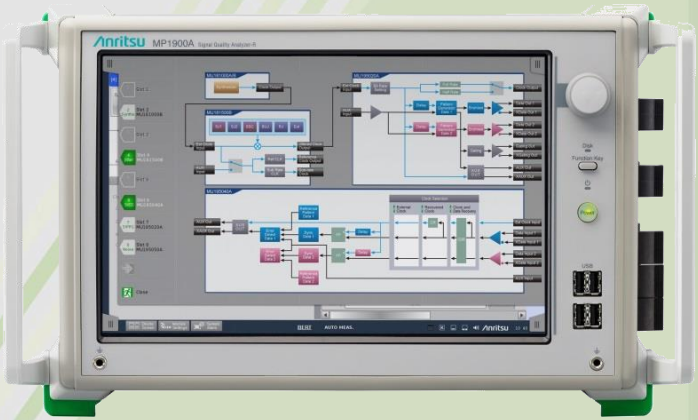
DDR5 Receiver Test Solution

Signal Quality Analyzer-R

MP1900A Series

SQA-R

CONFIDENTIAL



No. M3A-1SG220047

DDR5 Test Solution

Features

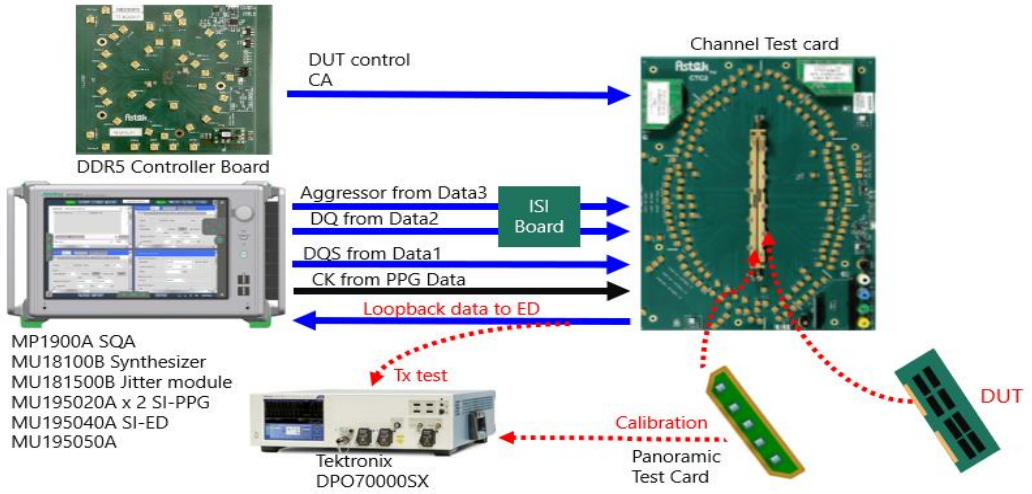
- All-in-one DDR5 and PCIe5 Receiver Test Support

  Wideband baud-rate operation from 2.4 Gbit/s to 32.1 Gbit/s with all-in-one module expansion supports PCIe5 (32 Gbit/s) and DDR5 (8.4 Gbit/s max.) to cut test equipment investment costs and save test benchtop space.

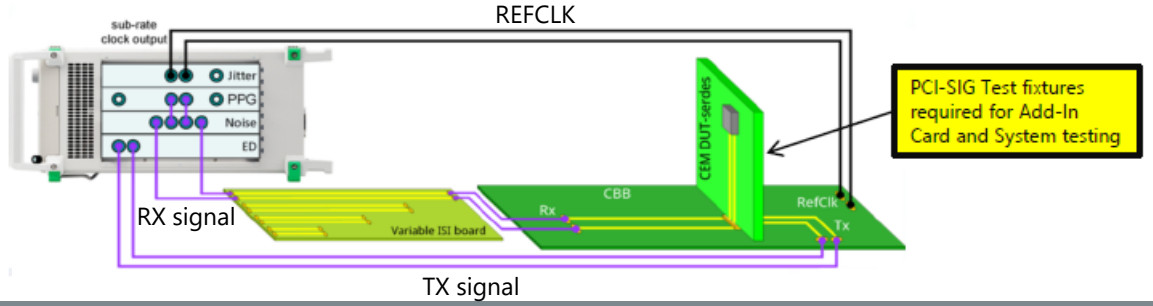
- Supports DDR5 Receiver Stress Tests

  Manual tests of both RDIMM DQ/DQS Voltage Sensitivity and DQS Jitter Sensitivity are supported. (Contact our business section about automation software support.)

DDR5 Setup



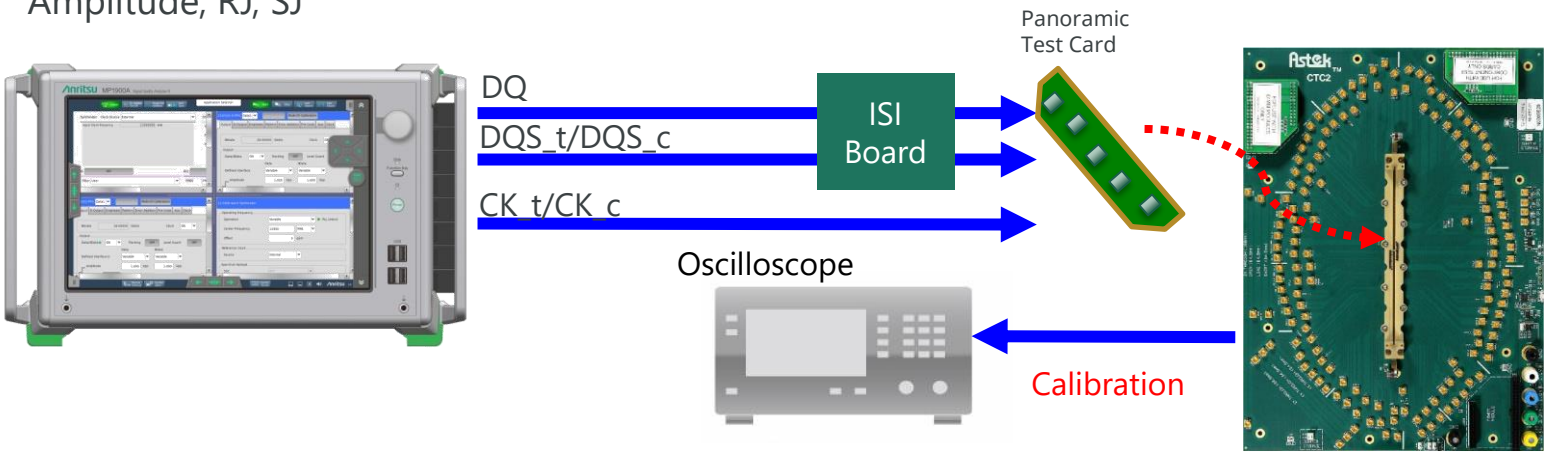
PCIe Gen5 Setup



DDR5 Receiver Test Solution

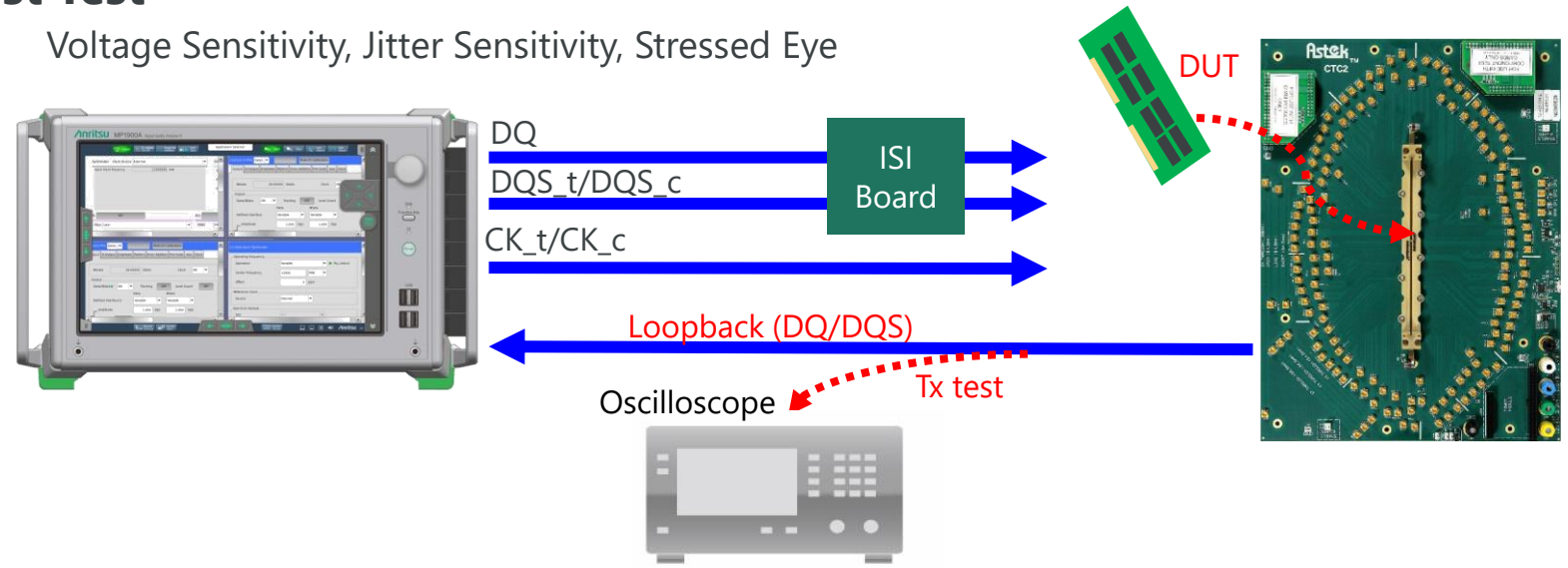
Calibration

Amplitude, RJ, SJ



Host Test

Voltage Sensitivity, Jitter Sensitivity, Stressed Eye

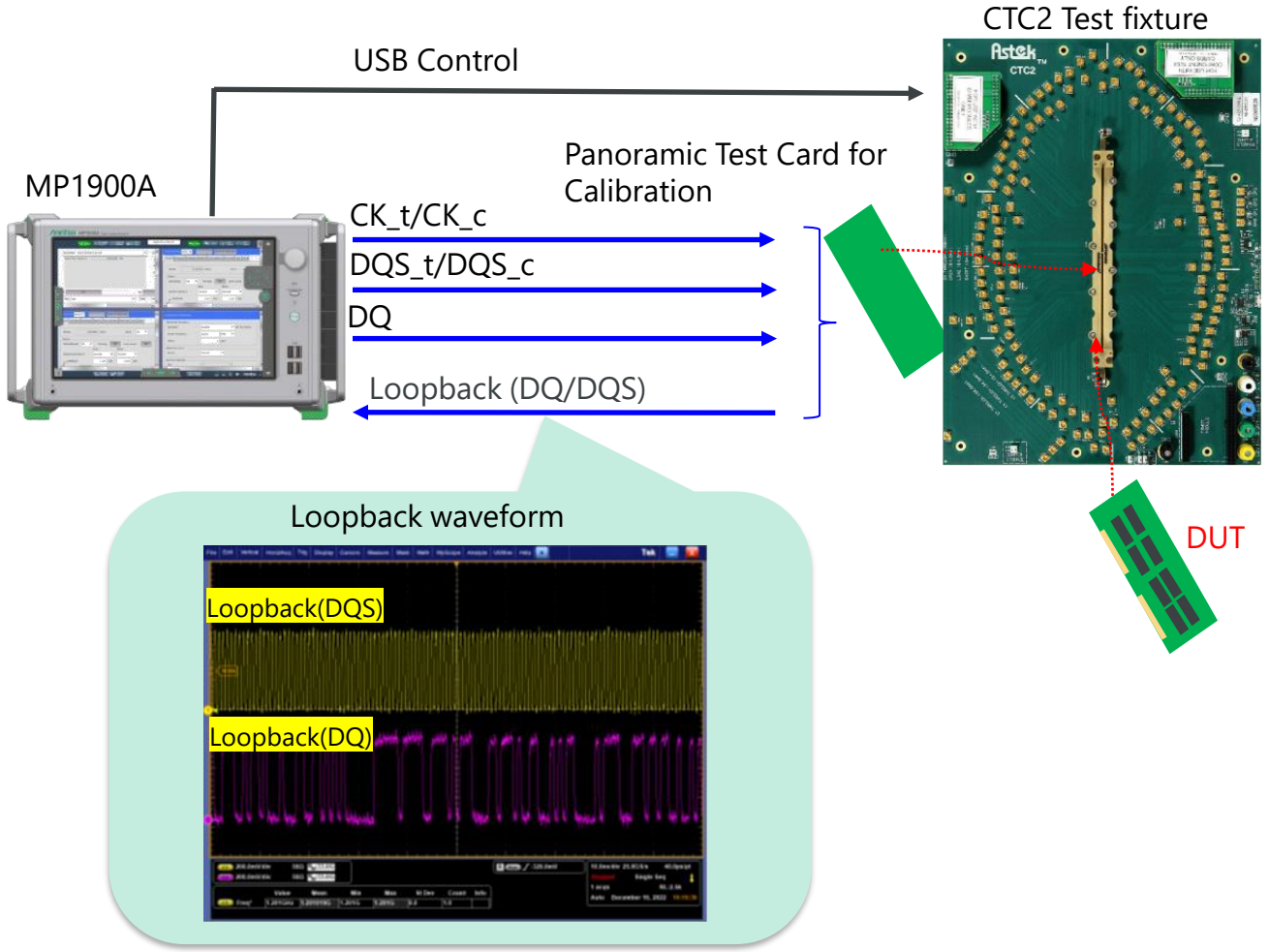


DDR5 Receiver Test Solution

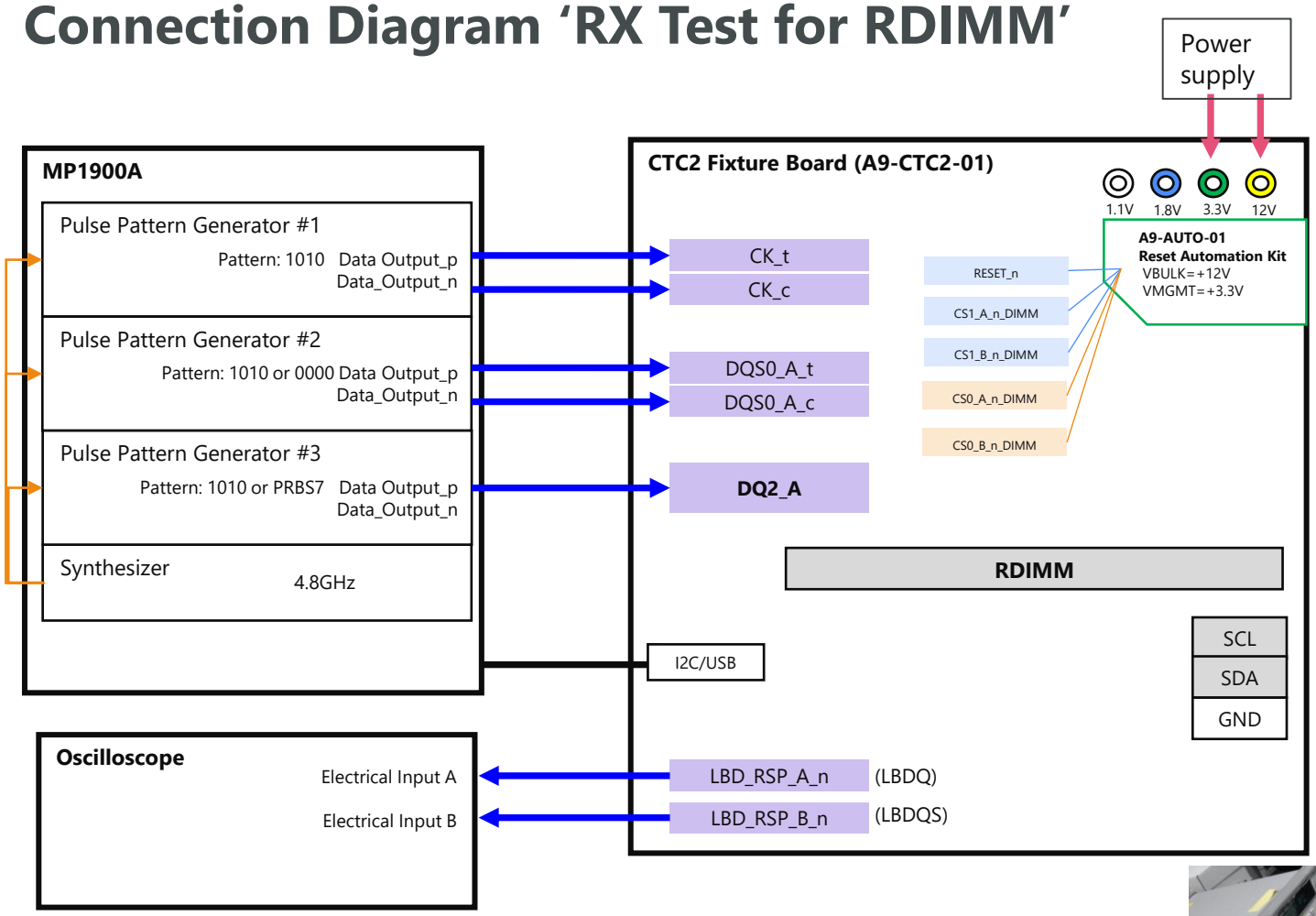
The following items can be measured by loading the required script from the MP1900A to the DUT for the RDIMM memory loopback settings.

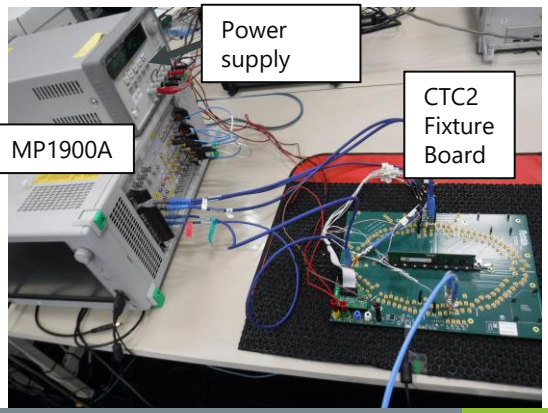
- Voltage sensitivity
- Jitter sensitivity
- Stressed Eye test

Modules for MP1900A
MU18100B Synthesizer
MU181500B Jitter
MU195020A SI-PPG x2
MU195040A SI-ED
MU195050A Noise



Connection Diagram 'RX Test for RDIMM'





Connection of MP1900A

Slot1/2
MU181000B

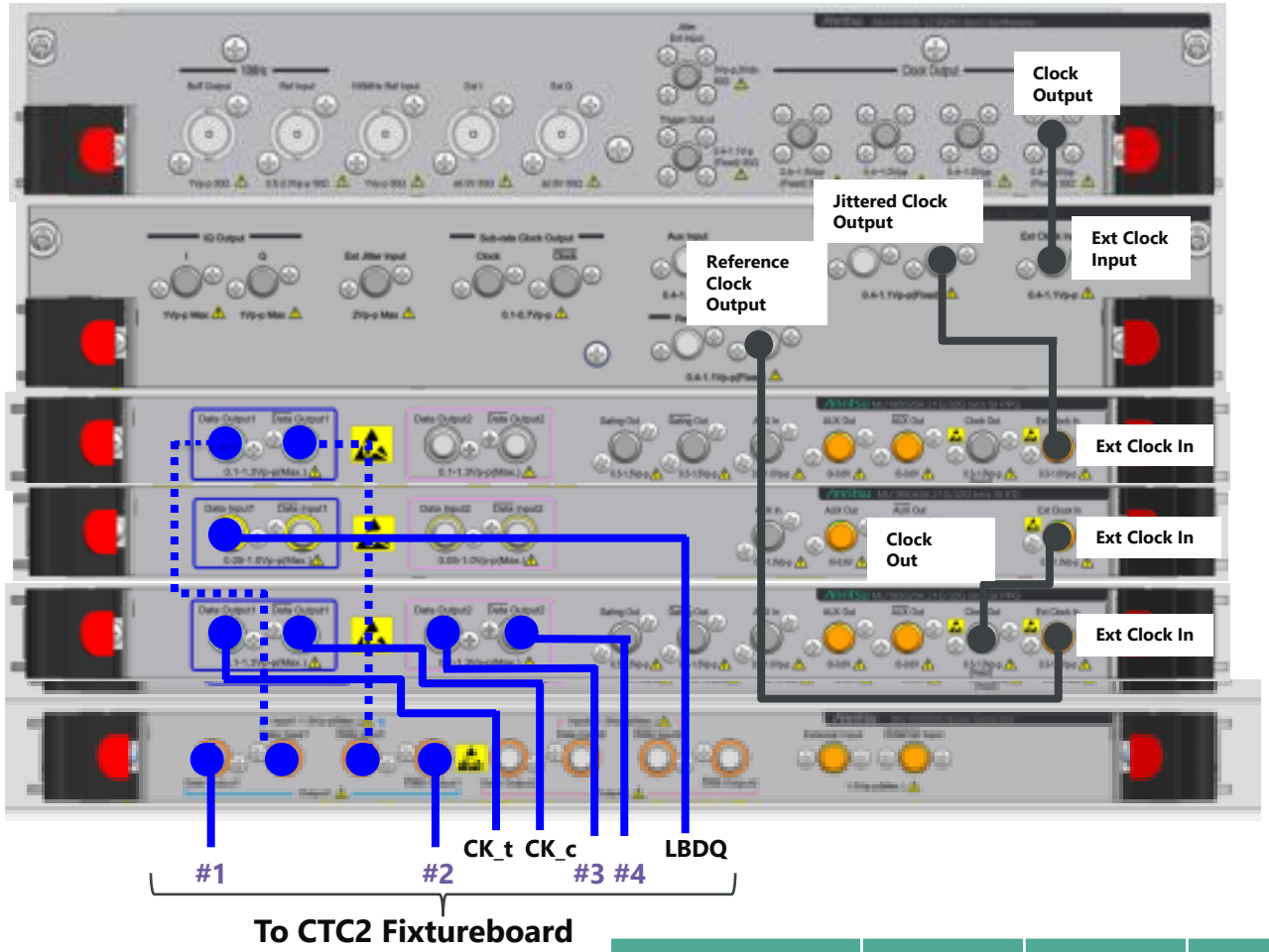
Slot3/4
MU181500B

Slot5
MU195020A

Slot6
MU195040A

Slot7
MU195020A

Slot8
MU195050A



Slot5 signal is added of jitter and noise.
The following changes are necessary according to DDR5 Test type.

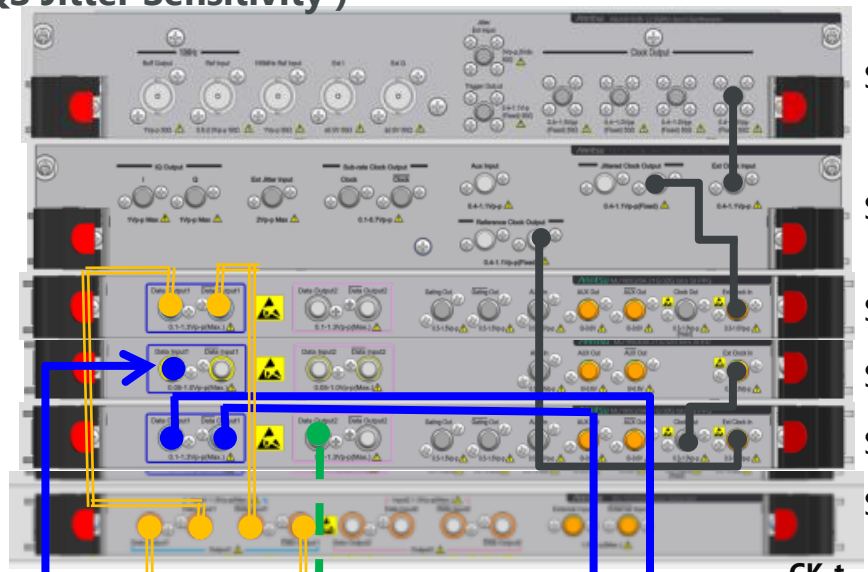
1: Change the connection between MP1900 and the Fixture board.
2: Change the setting of DQ/DQS according to DDR5 Test type.

DDR5 Test type	#1	#2	#3	#4
DQS Jitter Sensitivity	DQS_t	DQS_c	DQ	-
DQ Stressed Eye	DQ	-	DQS_t	DQS_c

Note:
DQ Voltage Sensitivity and DQS Voltage Sensitivity are available at both upper connection.

Connection Diagram between MP1900A and Fixture.

(DQS Jitter Sensitivity)



Slot1/2 **MU181000B**

Slot3/4 **MU181500B**

Slot5 **MU195020A**

Slot6 **MU195040A**

Slot7 **MU195020A**

Slot8 **MU195050A**

MP1900A Front pane USB-A port

Detail Connection is shown in next page.

CK_t

CK_c

DQS_c

DQS_t

DQ

CS1_A
CS1_B
Reset_n

CS0_A
CS0_B

A9-AUTO-01

LBDQ

LBDQS

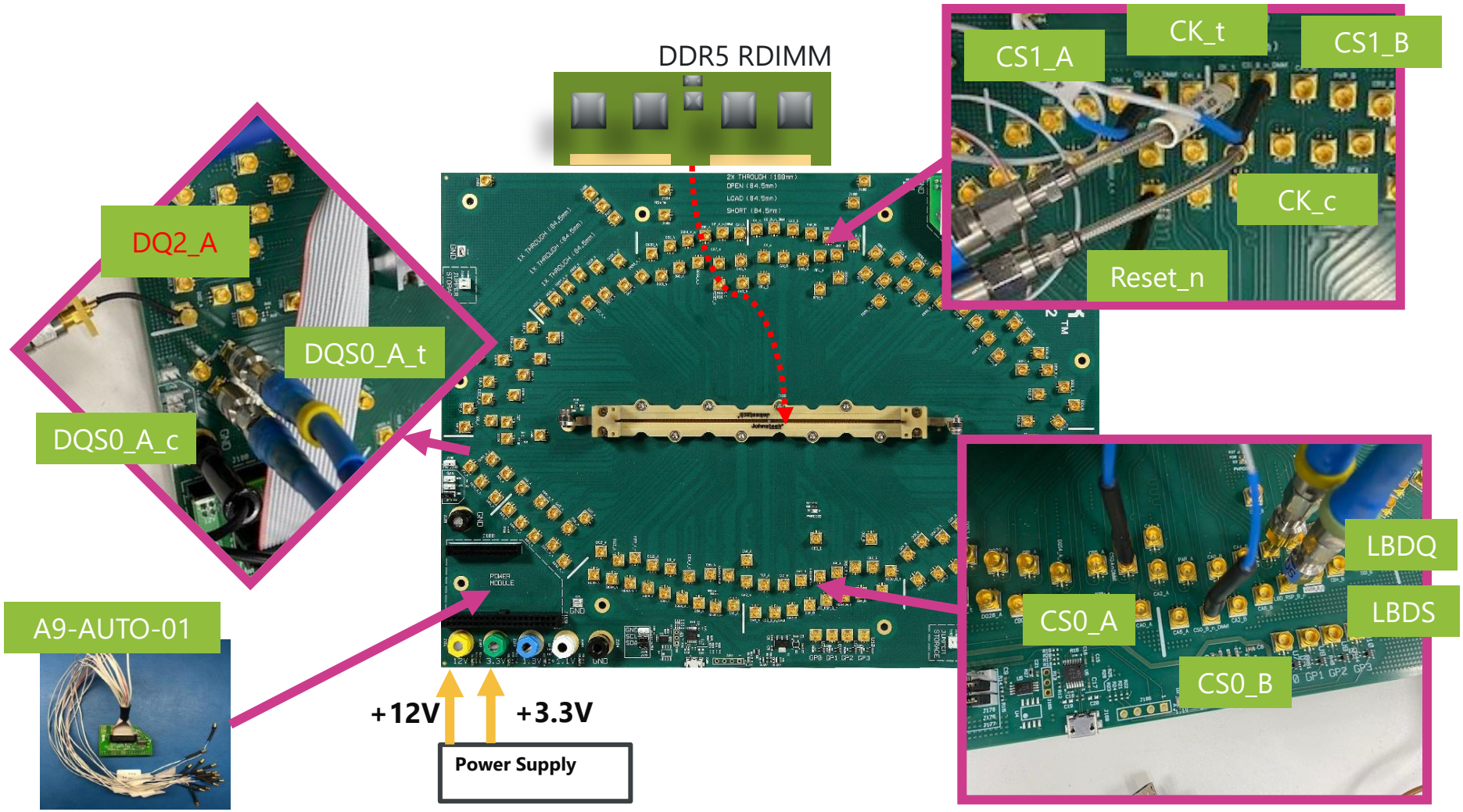
USB

A9-CTC2-01

+12V +3.3V GND

Power Supply

CTC2 Fixture Board Connection



DDR5 Receiver Test Recommended Configuration

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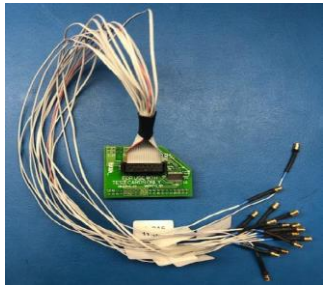
Model	Name	Qty (DDR5)	Qty (PCIe5)	Remarks
MP1900A	Signal Quality Analyzer-R	1	1	
MU181000B	12.5 GHz 4 Port Synthesizer	1	1	Opt-002 SSC Extension*1
MU181500B	Jitter Modulation Source	1	1	
MU195020A	21G/32G bit/s SI PPG	2	1	Opt-001 32G extension*1 Opt-020 2ch Data*4 Opt-021 2ch 10Tap Emphasis*4 Opt-031 2ch Data Delay*4 Opt-041 Variable ISI
MU195040A	21G/32G bit/s SI ED	1	1	Opt-001 32G extension*1 Opt-010 1ch ED Opt-011 1ch CTLE Opt-022 Clock Recovery
MU195050A	Noise Module	1	1	
MX183000A-PL001	PCIe Link Training	–	1	*1
MX183000A-PL025	PCIe5 Link Training	–	1	*1

Accessory *3

Model	Name	Qty	Remarks
A9-COMBO-01	Combo Test Card	1	Astek Inc*2
A9-CTC2-01	CTC2 Test Fixture	1	Astek Inc*2
A9-AUTO-01	Automation Kit	1	Astek Inc*2
A9-DIMM5-01	DDR5 Parametric Test Card	1	Astek Inc*2

*1 Required when including PCIe Gen5 solution *2 Purchase URL: https://www.astekcorp.com/products/test-measurement
*3 Also requires connection cables. *4 One of PPG mandatory (for DDR5)

Accessory



A9-AUTO-01
Automation Kit

- 16 SMP cables
- Reset, Chip Select, and Command/Address signals on the CTC2 to automatically perform reset sequencing of a DIMM

A9-CTC2-01
CTC2 Test Fixture

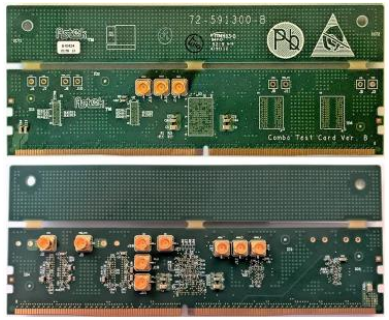
- All high-speed signals brought out to SMP connector
- All signals matched to within 1ps
- Supports DIMM testing
- 12V and 3.3V for DIMM mode

A9-COMBO-01
DDR5 Parametric Test Card

-All high-speed signals are brought out to SMP connectors

-Low speed signals are brought out to 50 mil headers

-VIN Bulk and VIN Management are brought out to 50 mil headers



A9-COMBO-01
Combo Test Card

- SMPs installed
- RCD, Memories, and Data Buffers must be provided by customer

Test Method

Items for Rx Test

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Item	Target pin	Contents
DQS Jitter Sensitivity	DQS	Jitter sensitivity
DQ Voltage Sensitivity	DQ	Voltage sensitivity
DQS Voltage Sensitivity	DQS	Voltage sensitivity
Stressed Eye	DQ	

DQS Jitter Sensitivity

- Set 111000 pattern on DQ(Non-ISI pattern)
- No added RJ or DCD on DQS
- Measure BER by changing DQS phase
- Do bathtub curve and report EW at BER 1E-9, extrapolate to BER 1E-16
- Check each 4phases
- Repeat all steps above, add RJ on DQS
- Repeat all steps above, add DCD on DQS
- Repeat all steps above, add RJ and DCD on DQS

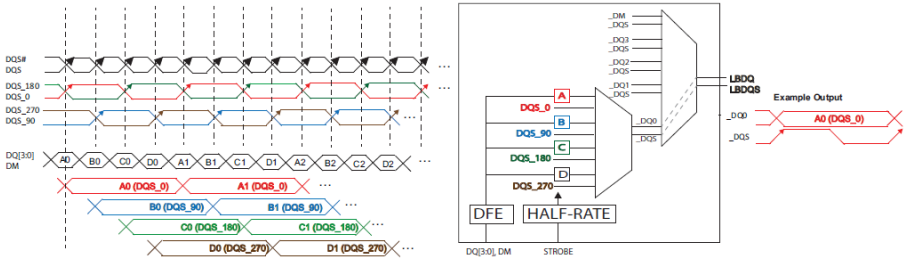


Figure 137 — Example of 4-Way Interleave Loopback Circuit on a x4 SDRAM

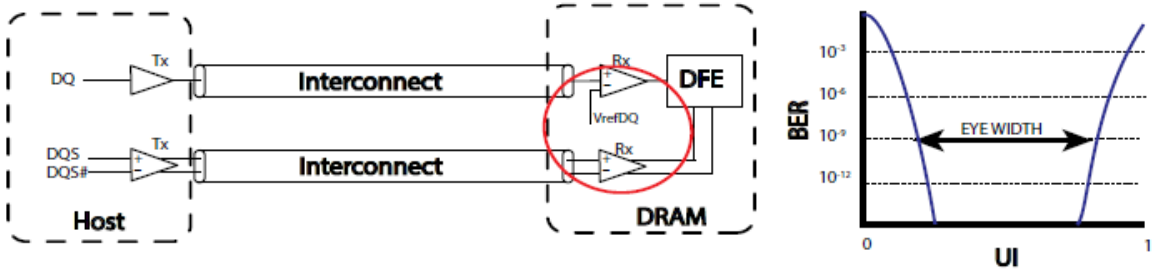


Figure 207 — SDRAM's Rx Forwarded Strobes for Jitter Sensitivity Testing

DQ Voltage Sensitivity

- Set 111000 pattern on DQ(Non-ISI pattern)
- No Rx Gain and DFE used for DUT
- Measure BER Bath-tub by changing DQ phase
- Change DQ Amplitude eye width margin goes to zero at BER 1E-16
- Check each 4phases

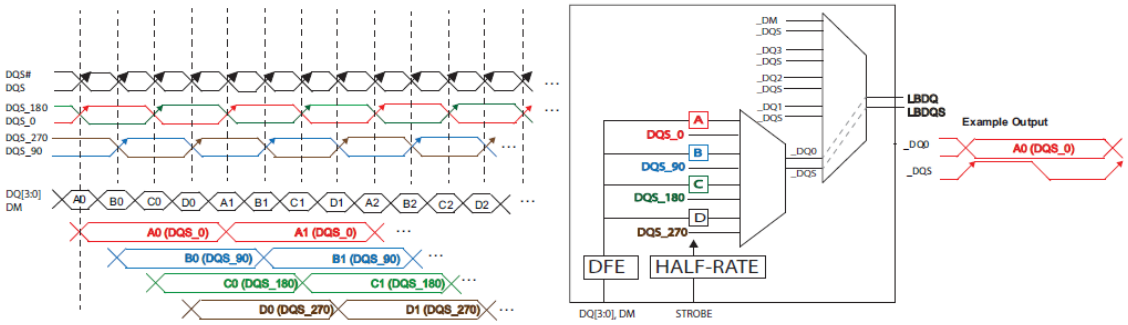
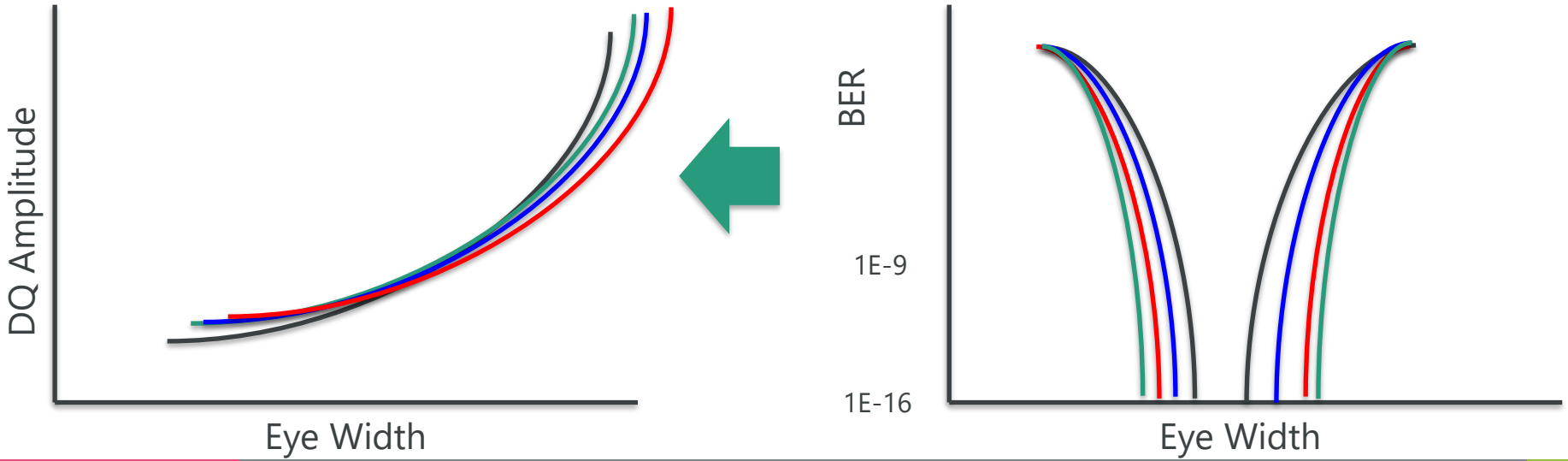
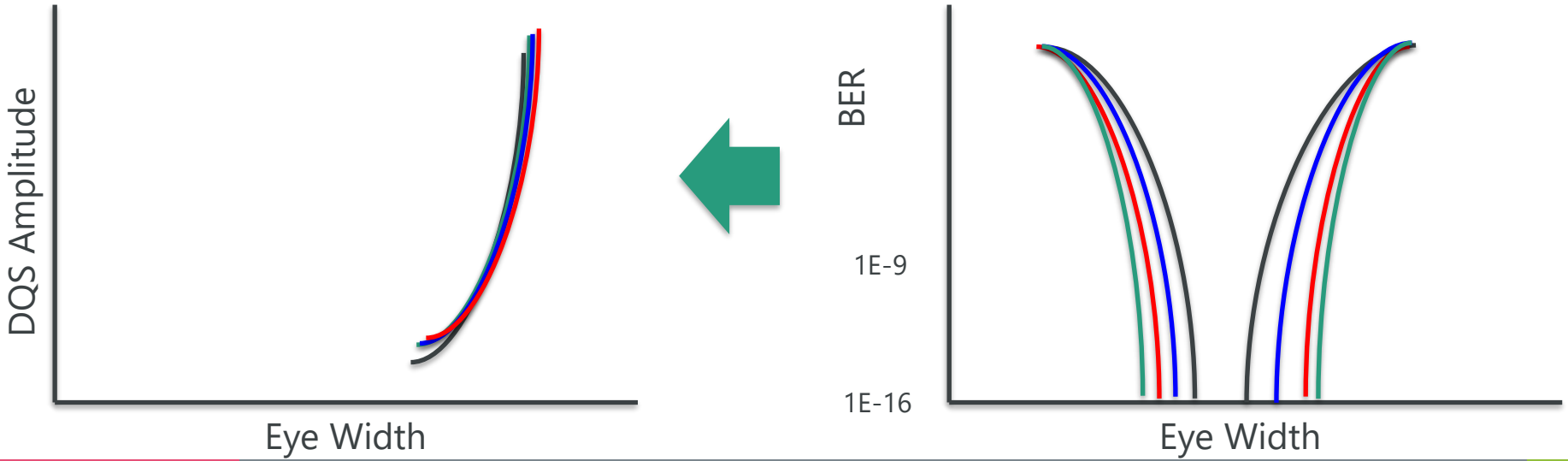


Figure 137 — Example of 4-Way Interleave Loopback Circuit on a x4 SDRAM



DQS Voltage Sensitivity

- Decrease DQS Amplitude, data lanes will no longer be able to accurately sample bits.
- DQS sensitivity is checked by Bath-tub until no extrapolated eye margin is present at BER 1E-16.
- Each phase may have different DQS sensitivity, so it is best to check all 4 phases



Stressed Eye

- Set 111000 pattern on DQ
- Calibrated jitter and noise stresses on DQ
- Measure BER by changing DQ phase
- Do bathtub curve and report EW at BER 1E-9, extrapolate to BER 1E-16
- Check each 4phases, plot composite bathtub curves

Parameter	Symbol	Value
Eye Height of stressed eye	EH	70 mV
Eye Width of stressed eye	EW	250 mUI
Vswing stress to meet EH	Vswing	600 mV
Injected sinusoidal jitter	SJ	450 mUI @200 MHz
Injected random jitter	RJ	40 mUI @10 MHz - 1 GHz
Injected voltage noise	Vnoise	125 mVp-p

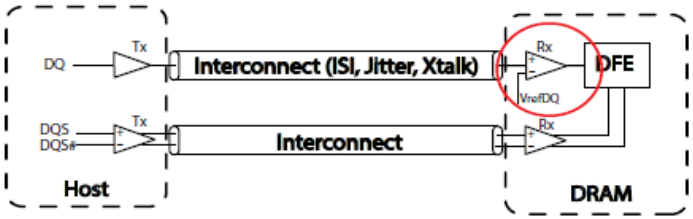


Figure 214 — Example of Rx Stressed Test Setup in the Presence of ISI, Jitter and Crosstalk

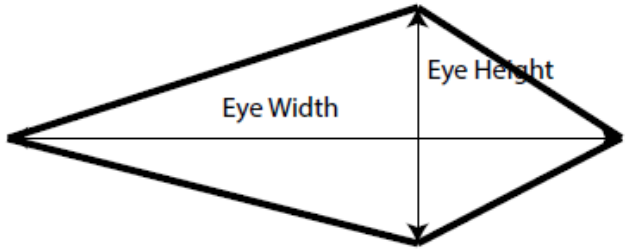


Figure 215 — Example of Rx Stressed Eye Height and Eye Width

Appendix

Ordering Information

Model	Name
MP1900A	Signal Quality Analyzer-R
MU181000B	12.5 GHz 4 Port Synthesizer
MU181000B-002	SSC Expansion
MU181500B	Jitter Modulation Source
MU195020A	21G/32G bit/s PPG
MU195020A-001	32G bit/s Extension
MU195020A-010	1ch Data Output
MU195020A-020	2ch Data Output
MU195020A-011	1ch 10Tap Emphasis
MU195020A-021	2ch 10Tap Emphasis
MU195020A-030	1ch Data Delay
MU195020A-031	2ch Data Delay
MU195020A-040	1ch Variable ISI
MU195020A-041	2ch Variable ISI
MU195020A-050*1	Sequence Editor Function
MU195020A-051*1	Sequence Editor Function PCIe 5 Extension
MU195040A	21G/32G bit/s ED
MU195040A-001	32Gbit/s Extension
MU195040A-010	1ch ED
MU195040A-020	2ch ED
MU195040A-011	1ch CTLE
MU195040A-021	2ch CTLE
MU195040A-022	Clock Recovery

Model	Name
MU195050A	Noise Generator
MU195050A-001	White Noise
MX183000A-PL001	Jitter Tolerance Test
MX183000A-PL011	PCIe Link Sequence
MX183000A-PL021	PCIe Link Training*2
MX183000A-PL025	PCIe5 Link Training*2
MX183000A-PL022	USB Link Training*3
MX183000A-PL023	USB 3.2 x 2 Link Training*3
MX183000A-PL031	DUT Error Counts Import

*1: MU195020A-050 supports PCIe1-4 and USB3.2 x1.
MU195020A-051 supports PCIe5.
Opt-050 required to add Opt-051.

*2: PL021 supports PCIe Gen1-4.
PL025 supports PCIe Gen5.
PL021 required to add PL025.

*3: PL022 supports USB3.2 x1.
PL023 supports USB3.2 x2.
PL022 required to add PL023.

Key Specifications

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• Signal Quality Analyzer-R MP1900A

Item	Specification
LCD	12.1" WXGA 1280 x 800
Remote Interface	GPIB, LAN
No. of Module Slots	8
External Equipment I/F	USB x6, VGA x1, HDMI x1
OS	Windows 10 IoT Enterprise
Power Supply	100 to 120/200 to 240 Vac, 50 to 60 Hz
Power Consumption	1350 VA max.
Dimensions/Mass	340 (W) x 222.5 (H) x 451 (D) mm/20 kg max. (exc. modules)

• 21G/32G bit/s SI ED MU195040A

Item	Specification
Operation Bit Rate	2.4 to 21 Gbit/s or 32.1 Gbit/s
No. of Channels	1 or 2
Input Amplitude	0.05 to 1.0 Vp-p (Single-End) 0.1 to 2.0 Vp-p (Differential)
Input Sensitivity	15 mV (Eye Height 28.1 Gbit/s)
CTLE	Peak Frequency: 14, 8, 4 GHz Gain: 0 to –12 dB
Clock Recovery	Supported with SSC input
PCIe/USB Link Training	Supported (MX183000A-PL021 (PCIe), MX183000A-PL022 (USB))
I/O Connectors	K (f)

• 21G/32G bit/s SI PPG MU195020A

Item	Specification
Operation Bit Rate	2.4 to 21 Gbit/s or 32.1 Gbit/s
No. of Channels	1 or 2
Output Amplitude	0.1 to 1.3 Vp-p (Single-end) 0.2 to 2.6 Vp-p (Differential)
Emphasis	10 Taps
Variable ISI	ISI, Channel Emulation functions
Tr/Tf (20% to 80%)	12 ps (typ.)
RJ	115 fs rms (typ.)
PCIe/USB Link Training	Supported (MX183000A-PL021 (PCIe), PL025 (PCIe 5), PL022 (USB))
I/O Connectors	K (f)

• Noise Generator MU195050A

Item	Specification
No. of Channels	2
Insertion Loss	–3 dB
CMI	0.1 to 1 GHz/1 to 6 GHz
DMI	2 to 10 GHz
White Noise	10 MHz to 10 GHz
Crest Factor	>5

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2023-8 MJM No. M3A-1SG220047-01